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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant	: David L. Chapek
Serial No.	: 09/605,293
Filed	: June 28, 2000
Title	: SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY
Docket No.	: MIO 0037 VA (96-0831.01)
Examiner	: N.D. Richards
Art Unit	: 2815

MAIL STOP APPEAL BRIEF - PATENTS
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NEW APPEAL BRIEF UNDER 37 CFR 41.37

This brief is being filed pursuant to the provisions of 37 CFR 41.37 in response to the Office Action received on October 4, 2005. That Office Action indicated that, in view of the Appeal Brief submitted on July 19, 2005, prosecution has been reopened for the purpose of reapplying a previous rejection, and adding new grounds of rejection. Pursuant to MPEP 1207.04, Applicant has elected to file a new appeal. A Notice of Appeal is being filed as a separate paper herewith.

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office at Reel 9159, Frame 0921.

Related Appeals and Interferences

Applicant knows of no currently pending related appeals or interferences that would have an effect on the outcome of this appeal.

Status of Claims

Claims 9-12 and 14 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

No amendments to the claims were filed after final rejection. All previous amendments have been entered.

Summary of Claimed Subject Matter

The present invention is directed to a semiconductor device or substrate which incorporates a layer of silicon dioxide which has been pretreated to provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. The pretreatment method includes implanting hydrogen ions into a layer of silicon dioxide by plasma source ion implantation and forming a layer of polycrystalline silicon on the layer of silicon dioxide such that the polycrystalline silicon layer is free of sputtered metal contaminants and has a smooth morphology.

By way of example and not limitation, the subject matter of independent claim 9 is shown in the embodiment illustrated in Fig. 1 and described at pages 7-10 of the specification. Layer 14 of silicon dioxide 16 is formed on a layer in a semiconductor substrate 12. After the layer is doped by plasma source ion implantation, a layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide to form a semiconductor device precursor which is free of sputtered metal contaminants.

By way of example and not limitation, the subject matter of independent claim 10 is shown in the embodiment illustrated in Fig. 2 and described at pages 10-11. A field effect transistor is provided which comprises a layer of silicon dioxide formed on a semiconductor substrate 52 and a gate oxide 54 and a source 56 and drain 58 formed on the semiconductor substrate. A layer of polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70.

The surface of the substrate 52 is pretreated with hydrogen ions as described above so that the subsequently formed layer 64 of polysilicon 66 has a smooth morphology and is free of sputtered metal contaminants.

By way of example and not limitation, the subject matter of independent claim 11 is shown in the embodiment illustrated in Fig. 3 and described at page 12. A memory array 100 is provided including a silicon dioxide layer formed on a semiconductor substrate and implanted with hydrogen ions as described above such that the layer is free of sputtered metal contaminants. A layer of polycrystalline silicon is formed over the silicon dioxide layer and has a smooth morphology. The memory array further includes a plurality of memory cells 102 arranged in rows and columns, each of which comprise at least one field effect transistor 50, a gate oxide for each of the field effect transistors, a source and drain for each of the field effect transistors, and a gate electrode for each of the field effect transistors.

By way of example and not limitation, the subject matter of independent claim 12 is shown in the embodiment illustrated in Fig. 4 and described at page 12. A semiconductor wafer W is provided including a layer of silicon dioxide formed on a semiconductor substrate 52 and implanted with hydrogen ions such that the layer is free of sputtered metal contaminants. A layer of polycrystalline silicon is formed over the silicon dioxide layer and has a smooth morphology. The semiconductor wafer W is divided into a plurality of die and comprises a repeating series of gate oxides formed on the semiconductor substrate, a repeating series of sources and drains for at least one field effect transistor formed on each of the plurality of die, and a repeating series of gate electrodes for the field effect transistor formed on each of the plurality of die.

By way of example and not limitation, the subject matter of independent claim 14 is shown in another embodiment illustrated in Fig. 5 and described at pages 13-14. A thin film transistor is provided in which a semiconductor substrate 202 formed from a layer of silicon dioxide, glass or quartz is doped with hydrogen ions as described above and is free of sputtered metal contaminants. A layer of polycrystalline silicon 206 is formed over at least a portion of the silicon dioxide layer, where the polycrystalline silicon layer has a smooth morphology. The thin film transistor 200 includes a layer of insulating material formed on at least a portion of the

polycrystalline silicon, a gate oxide formed from the layer of insulating material, a source and drain region formed in the polycrystalline silicon layer, and a gate electrode formed on the layer of insulating material.

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection for review on appeal are:

1) Claims 9-12 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

2) Claim 9 is rejected under 35 U.S.C. 102(a) as being anticipated by "Applicant's admitted prior art."

3) Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art."

4) Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "Applicant's admitted prior art."

Grouping of Claims

The Examiner has made four grounds of rejection, rejecting claims 9-12 and 14 under 35 U.S.C. 112, second paragraph, as being indefinite; rejecting claim 9 under 35 U.S.C. 102(a) as being anticipated by "Applicant's admitted prior art"; rejecting claims 10-12 under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art"; and rejecting claim 14 under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "Applicant's admitted prior art." The application contains five rejected independent claims, namely, claims 9, 10, 11, 12, and 14. Applicant submits that the claims do not stand or fall together. However, as all of the

independent claims contain the same rejected language, the arguments presented regarding the patentability of claim 9 are also representative of claims 10-12 and 14.

Argument

Rejection of claims 9-12 and 14 under 35 U.S.C. 112, second paragraph.

Claim 9

Claim 9 recites, inter alia, a semiconductor device precursor comprising a silicon dioxide layer on a semiconductor substrate, where the surface of the silicon dioxide layer has been doped with hydrogen ions deposited by a plasma ion implantation process and is free of sputtered metal contaminants. A layer of polycrystalline silicon is formed on the layer of silicon dioxide and has a smooth morphology.

In the Office Action mailed October 4, 2005, the Examiner indicated that the limitation "free" of sputtered metal contaminants is indefinite, asserting that in the context of the claims, "one of ordinary skill in the art would not know what level of contaminants is required to meet the limitation." The Examiner further asserted that the specification does not provide any objective standard for the relative term such that one of ordinary skill in the art would not know what level of contaminants is needed to be considered "free."

Applicant initially wishes to point out that this same rejection was made in a prior office action (mailed May 20, 2003), and that applicant submitted arguments in response to the rejection which resulted in the withdrawal of the rejection. Now, over two years later, after receiving multiple office actions for these claims that did not reject these claims on this basis, and after preparing and filing a brief on appeal that addressed other grounds of rejection, the Examiner has resurrected this old ground of rejection.

As previously pointed out to the Examiner, terms in a claim are to be read in light of the specification, the prior art, and how one skilled in the particular art would understand such terminology. MPEP §2173.02. Absolute precision and clarity are not required. Nor is there a requirement that numerical or percentage limitations be placed on claim terms. See, e.g., *In re Marosi*, 218 USPQ 289 (Fed. Cir. 1983) (phrase "essentially free of alkali metal" held definite

where specification provided general guidance; applicant not required to put a numerical value on the limitation). Applying those basic principles to the present application and claims, the specification defines the problem of metal contamination on page 1. More specifically, it is explained that a Kauffman ion source sputters metal from a grid and that such sputtered metal becomes implanted in the target (e.g., a layer of silicon dioxide), causing the target to become contaminated. See page 1, lines 17-23.

In addition, the specification teaches that using PSII reduces metal contamination on a target substrate because it does not use a metal grid. See page 10, lines 9-13. Thus, in light of the specification, it is evident to one of ordinary skill in the art that the phrase "free of sputtered metal contaminants" means that the layer of silicon dioxide (or semiconductor substrate in the case of claim 14) has no *sputtered* metal contaminants present. Neither the specification nor the claims recite that the layer is free from all metal contaminants (the claims recite "free from sputtered metal contaminants"). Moreover, the specification is clear that the use of PSII to implant hydrogen ions reduces metal contamination because it eliminates the metal grid that was present in prior art Kaufman ion implanting processes, thus eliminating *sputtered* metal contaminants from the surface of the layer. Applicant submits that claims 9-12 and 14 are definite and in compliance with §112.

Rejection under 35 U.S.C. 102(a) as anticipated by "Applicant's admitted prior art."

Claim 9

In the Office Action mailed October 4, 2005, the Examiner acknowledged that "Applicant's admitted prior art" does not explicitly disclose a layer of silicon dioxide which is "free of sputtered metal contaminants," but that "in light of the indefiniteness of the relative term 'free,' the limitation 'free of sputtered metal contaminants' is interpreted as meaning sufficiently free so as to operate." The Examiner further concluded that the silicon dioxide layer described in "Applicant's admitted prior art" which has been treated with a Kaufman ion source is free of sputtered metal contaminants. Applicant strongly disagrees.

By "Applicant's admitted prior art," the Examiner is referring to the discussion of the prior art Kaufman ion source implantation technique discussed at page 1, lines 12-22, of applicant's specification, which technique results in metal contamination on the surface of the target object. As pointed out above, the prior art Kaufman ion implanting processes cause contamination in the form of sputtered metal contaminants, while the use of PSII eliminates sputtered metal contaminants. When read in light of the specification, one skilled in the art would certainly not interpret the limitation "free of sputtered metal contaminants" as encompassing a silicon dioxide layer which *includes* sputtered metal contaminants as a result of treatment with a Kaufman ion source as described in "Applicant's admitted prior art." The Examiner has basically given clear and explicit claim terms a meaning that is contrary to the language which is recited, and then contends that, based on that misinterpretation, the claim reads on the prior art.

The Examiner's incorrect interpretation of Applicant's claims does not change the fact that the prior art method using a Kaufman ion source and a metal grid does not teach or suggest a layer of silicon dioxide which is "free of sputtered metal contaminants."

Claim 9 is clearly not anticipated by "Applicant's Admitted Prior Art."

Rejection under 35 U.S.C. 103(a) over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art"

Claim 10

Claim 10 recites a field effect transistor which includes a silicon dioxide layer having hydrogen ions implanted on its surface, a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology, and a gate oxide formed on the semiconductor substrate.

Burns et al. teach a field effect transistor including a source and drain, a layer of silicon dioxide, and a gate electrode formed of aluminum.

In the Office Action mailed October 4, 2005, the Examiner acknowledged that Burns et al. do not teach that their layer of silicon dioxide has hydrogen ions implanted therein or that their silicon dioxide layer is free of sputtered metal contaminants. However, the Examiner has

taken the position that "Applicant's admitted prior art" teaches a layer of silicon dioxide which is "free of sputtered metal contaminants" and that it would have been obvious to implant hydrogen ions into the silicon dioxide layer to obtain the invention of claim 10.

Applicant disagrees with the Examiner's reasoning as well as his conclusion. As applicant previously pointed out, "Applicant's admitted prior art" does not teach or suggest a method of ion implantation which produces a silicon dioxide layer which is free of sputtered metal contaminants. Rather, the prior art technique discussed at page 1 specifically teaches that metal from the metal grid used in the Kaufman ion source causes metal to become implanted in the target object, causing it to become contaminated. Accordingly, one skilled in the art would not look to a Kaufman ion source as a way to implant hydrogen ions in the silicon dioxide layer of Burns et al. Even if one did use a Kaufman ion source, the claimed field effect transistor would not result because such a technique would introduce sputtered metal contaminants on the silicon dioxide layer.

The Examiner's conclusion is based on his incorrect interpretation of the limitation "free of sputtered metal contaminants." The prior art Kaufman technique clearly teaches away from a process that produces a surface which is free of sputtered metal contaminants. In combining the teachings of the references, the Examiner cannot ignore the fact that the prior art Kaufman method does not teach a treatment which eliminates sputtered metal contaminants, and provides no expectation of a successful solution of that problem.

Claim 10 is clearly patentable over the cited references.

Claim 11

Claim 11 recites a memory array including a semiconductor substrate with a silicon dioxide layer on the substrate having hydrogen ions implanted on its surface (which silicon dioxide layer is free of sputtered metal contaminants), and a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology. In the Office Action mailed October 4, 2005, the Examiner asserts that, based on the combination of Burns et al. and "Applicant's admitted prior art," the gate oxide for each transistor "would be formed of the silicon dioxide having hydrogen atoms implanted therein."

Again, there is no teaching or suggestion that the prior art Kaufman technique produces a silicon dioxide layer which is free of sputtered metal contaminants. To the contrary, sputtered metal contaminants are produced. Nor is there any teaching or suggestion in the references which would motivate one skilled in the art to combine their teachings to make the claimed memory array, nor do the cited references provide any expectation of success. Claim 11 is clearly patentable over the cited references.

Claim 12

Claim 12 recites a semiconductor wafer including a semiconductor substrate, with a silicon dioxide layer on the substrate having hydrogen ions implanted on its surface (which silicon dioxide layer is free of sputtered metal contaminants), and a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology. The Examiner asserts that one of ordinary skill in the art would have formed the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die as recited in claim 12. Again, the Examiner has failed to cite any reference, alone or in combination, which teaches or suggests a semiconductor wafer in which the layer of silicon dioxide formed on the semiconductor substrate has been implanted with hydrogen ions on its surface which are free of sputtered metal contaminants as claimed. Claim 12 is clearly patentable over the cited references.

Rejection under 35 U.S.C. 103(a) over Murata et al. in view of Applicant's admitted prior art

Claim 14

Claim 14 recites a thin film transistor comprising a semiconductor substrate formed from silicon dioxide, quartz, or glass which has been implanted on its surface with hydrogen ions by plasma source ion implantation such that the substrate is free of sputtered metal contaminants, and a layer of polycrystalline formed on the substrate having a smooth morphology. Murata et al. teach a method of forming a thin film transistor on a glass substrate where hydrogen ions and

metal ions are simultaneously implanted through a capping film and polysilicon film using a plasma source.

In the Office Action mailed October 4, 2005, the Examiner admitted that Murata et al. do not teach a substrate having hydrogen ions implanted therein which is free of metal contaminants as claimed, but reasons that it would have been obvious to implant hydrogen ions into the glass substrate of Murata et al. based on the teachings of "Applicant's admitted prior art" to achieve a substrate which is free of metal contaminants. However, as pointed out above, the prior art Kaufman ion technique results in a silicon dioxide layer having sputtered metal contaminants, not a layer which is "free of sputtered metal contaminants" as claimed.

Further, Murata et al. do not address the same problem as applicant, nor do they provide a solution to that problem. Rather, Murata et al. teach the implantation of hydrogen ions and metal ions into a semiconductor film for the purpose of obtaining a film having low resistivity. See col. 3, lines 27-37. Nothing in the references provides motivation for preparing the glass surface of the substrate of Murata et al. such that it is free of metal contaminants and such that the subsequent deposition of a polycrystalline silicon layer has a smooth morphology as claimed. There is no motivation for one skilled in the art to use a Kaufman ion source implantation technique in Murata as such a technique would result in sputtered metal contamination.

Claim 14 is clearly patentable over the cited combination of references.

Conclusion

Claims 9-12 and 14 are in compliance with 35 U.S.C. 112, second paragraph, as the limitation "free of sputtered metal contaminants" is clear and definite when read in light of the specification.

Claim 9 is clearly not anticipated by "Applicant's admitted prior art," which describes a technique which results in sputtered metal contamination on a target surface, not a surface which is free of sputtered metal contaminants as claimed.

Finally, the Examiner has failed to establish a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of references. No motivation or suggestion exists to combine the teachings of the

cited references as none of the references teaches or suggests providing hydrogen ions implanted on the surface of a silicon dioxide substrate such that the substrate is free of sputtered metal contaminants as claimed.

The Board is requested to reverse the rejections of claims 9-12 and 14 in their entirety.

Respectfully submitted,

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CLAIMS APPENDIX

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, the surface of said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of sputtered metal contaminants; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, the surface of said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, wherein hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor;

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series of sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of sources and drains being formed on said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, the surface of said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of an insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide formed from said layer of insulating material;

a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE